Code No: 155AA **R18**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**B. Tech III Year I Semester Examinations, March - 2021**
**ADVANCED COMPUTER ARCHITECTURE**
**(Computer Science and Engineering)**

**Time: 3 Hours** **Max. Marks: 75**

**Answer any five questions**
**All questions carry equal marks**
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1.a) Discuss the evolution of computer architecture.
b) Differentiate between implicit parallelism and explicit parallelism.
c) Describe NUMA model for shared memory multiprocessor. [5+5+5]

2.a) Give the Bell's taxonomy of MIMD computers.
b) Describe an operational model of an SIMD computer.
c) Define the five types of data dependence. [5+5+5]

3.a) Make a comparison of Amdahl's law and Gustafson's law as speed up performance models.
b) Identify the basic metrics affecting the scalability of a computer system for a given application. [8+7]

4.a) Distinguish between RISC and CISC scalar processors.
b) Describe the architecture of a typical VLIW processor and instruction format. [8+7]

5.a) What is meant by bus arbitration? Explain Daisy-chain bus arbitration.
b) Describe Total Store Order weak consistency model used in SPARC architecture.[7+8]

6.a) What is the importance of dynamic instruction scheduling? Explain Tomasulo's algorithm.
b) Illustrate the schematic design of a cross point switch in a crossbar network. [8+7]

7.a) Explain the building blocks and the application paradigms of the Connection Machine (CM) -5.
b) Discuss the routing schemes followed in a multi computer network and analyze their communication latencies. [7+8]

8.a) Describe any two latency hiding techniques for enhancing scalability and programmability.
b) Explain the message-driven processor architecture. [8+7]

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